TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	10/609,216
Filing Date	June 26, 2003
First Named Inventor	Karl H. Mauritz
Art Unit	2186
Examiner Name	Patel, Hetul B.
Total Number of Pages in This Submission	15
Attorney Docket Number	42P16326

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
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- [ ] CD, Number of CD(s)
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- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) *(please identify below):*

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Gordon R. Lindeen III, Reg. No. 33,192 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	August 14, 2006

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	**Debbie Casias**		
Signature	Debbie Casias	Date	**August 14, 2006**

FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	500.00

Complete if Known	
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First Named Inventor	Karl H. Mauritz
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Art Unit	2186
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METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below
☐ Charge fee(s) indicated below, except for the filing fee
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☒ Credit any overpayments

FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
				Other fee (specify) _____	
				SUBTOTAL (2)	($) 500.00

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Gordon R. Lindeen III	Registration No. (Attorney/Agent)	33,192	Telephone	(303) 740-1980
Signature				Date	08/14/06

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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ZFW
AF

Docket No.: 42390P16326 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of:		
	Karl H. Mauritz	
Serial No.:	10/609,216	Art Unit: 2186
Filed:	June 26, 2003	
		Examiner: Patel, Hetul B.
For:	Electrical Solution to Enable High-Speed Memory Interfaces	

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313

AMENDED APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicants (hereafter "Appellants") hereby submit this Brief in support of its appeal from a final decision by the Examiner, mailed March 14, 2006 in the above-captioned case. Appellants respectfully request consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

An oral hearing is not desired.

08/21/2006 EFLORES 00000056 10609216
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TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052-8119.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences that are related to, will directly affect, will be directly affected by, or have a bearing on the Board's decision in the present appeal.

III. STATUS OF THE CLAIMS

Claims 1-30 are currently pending in this application. No claims have been canceled. No claims have been allowed. All pending claims were rejected in the final Office action mailed March 14, 2006 and are the subject of this appeal.

Claims 1-30 stand rejected under 35 U.S.C. §112 as not described in the original specification.

Claims 1, 4, 7, 8, 14, 17, 19, 20, and 21 stand rejected under 35 U.S.C. §102(e) as anticipated.

The remaining claims stand rejected as obvious, but these rejections rely on the anticipation rejection.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed on March 14, 2006, rejecting claims 1-30, Appellants timely filed a Notice of Appeal on June 14, 2006.

A copy of all claims on appeal is attached hereto as Appendix A.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 1 refers to a circuit with the following elements:

a plurality of memory modules (item 204, Page 9, line16-Page 10, line 8);

a memory controller coupled to the plurality of memory modules (item 112, Page 9, line16-Page 10, line 8);

a resistive bus splitter (item 211, 213, 215, Page 9, line16-Page 10, line 8) coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller, the resistive bus splitter having a specific resistance for each memory module (items Rs, Page 10, lines 11-19, Page 13, lines 16-17); and

a plurality of terminators to reduce signal reflections corresponding to the split signals (Page 11, lines 2-10, Page 15, lines 9-10) .

Claim 14 is directed to operating a circuit like that of Claim 1 and the same portions of the specification apply.

Claim 21 is directed to a computer system as follows:

a central processing unit (CPU) (item 102 Page 6, line 15-Page 7, line 6);

a graphics accelerator (item 130, Page 7, line 16-Page 8, line8) coupled to the CPU to generate an image;

a plurality of memory modules (item 115, 204 Page 7, lines 9-15, Page 9, line16-Page 10, line 8);

a memory controller (item 112, Page 7, line 9, Page 9, line16-Page 10, line 8); coupled to the plurality of memory modules and the CPU;

a resistive bus splitter (this is similar to that of Claim 1, discussed above); and

a plurality of terminators (also similar to that of Claim 1).

The remaining claims are dependent claims.

One of the problems addressed by Claim 1 is described in the present application in paragraphs 5 and 6 as follows: dual in-line memory modules (DIMMs) are generally

routed in parallel (i.e., with one signal visiting each DIMM). As the signal travels from chipset to DIMM then to another DIMM, each DIMM represents an electrical discontinuity (or impedance discontinuity), which degrades the signal, in part, because a portion of the wave reflects back to the chipset (also called a reflection) and another portion is passed to the next DIMM.

The signal reflection problem is further exasperated in multiple DIMM configurations because each DIMM may generate an additional reflection for each signal line it shares with other DIMMs. Also, as the data rates increase, the detrimental affects become increasingly difficult to manage.

VI. GROUNDS OF REJECTION

A. Whether the resistors shown in Figures 2 and 4 support a limitation of "a resistive bus splitter having a specific resistance for each memory module" under 35 U.S.C. §112.

B. Whether the reference, having no indication of how a connection is made, anticipates the specific limitation of "a resistive bus splitter ... to split signals communicated between the plurality of memory modules and the memory controller, the resistive bus splitter having a specific resistance for each memory module" under 35 U.S.C. §102(e).

VII. ARGUMENT

A. Introduction

While the arguments below are directed only to Claim 1, they are believed to apply also to the other pending claims.

B. The Resistors Rs Clearly show a Resistance Sufficient to Support a Claim to "Having a Specific Resistance" as Recited in Claim 1.

Claims 1-30 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Examiner would appear to suggest that there is no support for a specific resistance in the originally filed application and points to the discussion of impedance in paragraphs 24 and 25 of the specification.

Applicants are willing to amend the claims from "resistance" to "impedance" if that will overcome the rejection. Such an amendment was proffered in an amendment after final, however, the Examiner refused to enter the amendment and refused to withdraw the rejection.

Referring to Figure 2, it specifically shows a resistor between each DIMM connector and the Controller. These resistors will have a resistance as recited in the claim. This resistance is characterized in paragraph 22 (page 10, line 11). On page 13, lines 17-18 it is stated that the bus splitters are resistive. Applicants respectfully submit that these teaching in the application provide ample support for the splitter having a specific resistance for each memory module.

The Examiner argues that only impedance is taught in paragraphs 24 and 25 and that this does not support resistance because impedance depends also on frequency. While impedance may depend on frequency it also depends on resistance. While the impedance for each memory module will change with frequency, the resistance will not. Since embodiments of the present invention may be operated at a variety of different

frequencies, it is more convenient to refer to the resistance. The resistors in the drawings clearly suggest, a particular resistance for each module.

C. Absent any Teaching of How Signals are Distributed "a Resistive Bus Splitter Having a Specific Resistance (or Impedance) for Each Memory Module" as Recited in Claim 1 is not Anticipated.

The Examiner has rejected claims 1, 4, 7-8, 14, 17 and 20-21 under 35 U.S.C. §102 (e) as being anticipated by Morris, U.S. Patent No. 6,862,185 ("Morris"). The Examiner asserts that Morris shows memory modules 201, and a memory controller 207. The memory bus splitter are not shown, but the Examiner suggests that these are embedded in the memory board 203 to split the signals to the many connectors 202. Applicants suggest that since Morris makes no teaching or suggestion to the contrary, it should be assumed that the memory bus of Morris is completely conventional. In other words, the same bus lines connect in parallel to all of the memory chips in the memory modules without any splitter. This is the conventional approach described in the BACKGROUND section of the present application.

Referring to Claim 1, for example, it recites, *inter alia*:

"a resistive bus splitter coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller, the resistive bus splitter having a specific resistance for each memory module."

As shown in Figure 2 of the present application, each splitter 211, 213, 215 not only splits the signals communicated between the memory modules 204 and the memory controller 112, they also have a specific resistance for each memory module, shown in Figure 2 as Rs and indicated by the resistors on either side of the split. The specification at paragraph 22 provides some examples of how the resistances might be determined.

Morris simply has no information at all about how any busses connect any of the components together.

Accordingly Claim 1 is believed to be allowable over the reference. Claims 14 and 27 contain similar recitations and are believed to be allowable for the same reasons discussed above. The remaining claims are believed to be allowable also on similar grounds and for the particular recitations set forth expressly in each claim, respectively.

VIII. CONCLUSION

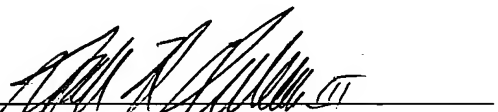
Appellants respectfully submit that all the appealed claims in this application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

Please charge any shortages and credit any overpayment to out Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: August 14, 2006



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APPENDIX OF CLAIMS (37 C.F.R. § 1.192(c)(7))

1. A circuit comprising:

a plurality of memory modules;

a memory controller coupled to the plurality of memory modules;

a resistive bus splitter coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller, the resistive bus splitter having a specific resistance for each memory module; and

a plurality of terminators to reduce signal reflections corresponding to the split signals.

2. The circuit of claim 1 wherein the plurality of terminators are embedded in each of the plurality of memory modules.

3. The circuit of claim 1 wherein the plurality of terminators are embedded in the memory controller.

4. The circuit of claim 1 wherein the memory modules are dual in-line memory modules (DIMMs).

5. The circuit of claim 1 further including a reference voltage generator to generate a reference voltage corresponding to a memory chip voltage.

6. The circuit of claim 5 wherein the reference voltage is provided to the plurality of memory modules and the memory controller.

7. The circuit of claim 1 wherein the resistive bus splitter includes miniature integrated resistor packs.

8. The circuit of claim 1 further including a plurality of memory expander chips (MXCs) coupled between the resistive bus splitter and the plurality of memory modules.

9. The circuit of claim 8 wherein the plurality of MXCs include a micro-controller to perform tasks locally.

10. The circuit of claim 8 wherein each of the plurality of MXCs include a built in bi-directional cache to decrease latency and increase throughput efficiency.

11. The circuit of claim 8 wherein a data rate between the memory controller and the plurality of MXCs runs at a relatively higher bandwidth than that of directly supported DIMMs.

12. The circuit of claim 8 wherein each of the plurality of MXCs include functionality selected from a group comprising local refresh generation, dynamic address space re-mapping, access re-ordering, access coalescing, memory power-on self-test (POST), and local management of open pages.

13. The circuit of claim 8 wherein a portion of the plurality of MXCs are coupled to each other in series.

14. A method comprising:

sending address signals from a memory controller to a plurality of memory modules through a resistive bus splitter;

splitting the address signals communicated between the plurality of memory modules and the memory controller at the resistive bus splitter;

providing a specific resistance to the address signals for each memory module at the resistive bus splitter; and

terminating the address signals to reduce signal reflections corresponding to the split signals.

15. The method of claim 14 wherein terminating comprises terminating at terminators embedded in each of the plurality of memory modules.

16. The method of claim 14 wherein terminating comprises terminating at terminators embedded in the memory controller.

17. The method of claim 14 wherein the memory modules are dual in-line memory modules (DIMMs).

18. The method of claim 14 further including generating a reference voltage corresponding to a memory chip voltage and providing the reference voltage to the plurality of memory modules and to the memory controller.

19. The method of claim 18 wherein the resistive bus splitter includes a miniature resistive splitter on a PCB.

20. The method of claim 14 wherein the resistive bus splitter includes miniature integrated resistor packs.

21. The method of claim 14 sending address signals further includes sending the address signals through a plurality of memory expander chips (MXCs) between the resistive bus splitter and the plurality of memory modules.

22. The method of claim 21 wherein the plurality of MXCs enable access to relatively larger memory arrays.

23. The method of claim 21 wherein each of the plurality of MXCs include one or more items selected from a list comprising a micro-controller to perform tasks

locally and a built in bi-directional cache to decrease latency and increase throughput efficiency.

24. The method of claim 21 wherein a data rate between the memory controller and the plurality of MXCs runs at a relatively higher bandwidth than that of directly supported DIMMs.

25. The method of claim 21 wherein each of the plurality of MXCs include functionality selected from a group comprising local refresh generation, dynamic address space re-mapping, access re-ordering, access coalescing, memory power-on self-test (POST), and local management of open pages.

26. The method of claim 21 wherein a portion of the plurality of MXCs are coupled to each other in series.

27. A computer system comprising:

a central processing unit (CPU);

a graphics accelerator coupled to the CPU to generate an image;

a plurality of memory modules;

a memory controller coupled to the plurality of memory modules and the CPU;

a resistive bus splitter coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller, the resistive bus splitter having a specific resistance for each memory module; and

a plurality of terminators to reduce signal reflections corresponding to the split signals.

28. The computer system of claim 27 wherein the resistive bus splitter includes miniature integrated resistor packs.

29. The computer system of claim 27 further including a-plurality of memory expander chips coupled between the resistive bus splitter and the plurality of memory modules to perform memory functions independent of the memory controller.

30. The computer system of claim 29 wherein the memory expander chip functions include at least one of refresh, dynamic address space re-mapping and memory power-on self-test (POST).

XI. EVIDENCE APPENDIX

None.

XII. RELATED PROCEEDINGS APPENDIX

None.